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Correlated Positive Charges and Deep Donor and Acceptor "Border" traps in Si and 4H-SiC MOS Devices

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Abstract: *4H-SiC (0001) oriented surface compares to the Si (111) surface in terms of planar density of atoms. The positive charge and deep donor and acceptor "Border" trap densities in the MOS devices on the two surfaces correlate to each other with the charge and trap density in the 4H-SiC MOS devices being three times those in the Si MOS devices at 12 x 10^{11}/cm^{2}in the wet oxidised/wet re-oxidised/Ar annealed sample. The N_f values in the p-type and n-type devices on Si-face of 4H-SiC create a window of 36 x 10^{11}/cm^2 as the charge density. Moving the window to the left through processing increases the leakage current and lowers the oxide breakdown field. Moving the window to the right increases the density of near interface traps (NITs) that reduces the surface mobility of the n-channel MOSFET. A high value of interface trap density implies a higher density of carbon atoms at the SiC/SiO_2 interface. The window of ΔN_f could be related to the density of P_{bC} centres on 4H-SiC which is found to be 30-40 x 10^{11}/cm^2. One-third of the window represents density of E' centres near the SiO_2/Si(111) interface at 12 x 10^{11}/cm^2 because of absence of carbon and indicates better interface abruptness.*

Keywords: *MOS Devices, Silicon, Silicon Carbide, Planar density, Donor and Acceptor traps*

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I. Introduction

This article is intended to highlight correlation between electrically inactive positive fixed charge densities and border trap densities in the Si/SiO_2 and the 4H-SiC/SiO_2 systems. It is found that the fixed positive charge density N_f, in n-type and p-type MOS devices on Si-face of 4H-SiC compound semiconductor having (0001) orientation is 12 x 10^{11}/cm^2 and the border trap density of deep acceptor traps or density of near interface traps D_{NIT}, is also 12 x 10^{11}/cm^{2}eV after wet re-oxidation at 950^{o}C for 3 hrs of the dry or wet grown thermal oxide [1]. These charge and trap densities are correlated to the charge and trap densities in the Si/SiO_2 system under similar processing conditions such as the final temperature of 950^{o}C or 920^{o}C. Carbon, having two less electrons compared to oxygen, adds positive charge to the Si-C-O bonded molecules, making the increase in densities three times in 4H-SiC/SiO_2 MOS devices. The positive charge density have been found to be 4 x 10^{11}/cm^2 for the dry or wet oxide on n-or p-type MOS devices on Si (111) surface and fast pulled out from the wet oxidising ambient [2], and the lower bound on the border trap density in the Si MOS devices is found to be ~3 x 10^{11}/cm^{2}eV [3-4]. These densities are three times less than those in the 4H-SiC/SiO_2system due to the absence of carbon, completely correlating the charges in the two systems.

II. Theory

Silicon has a diamond lattice structure that belongs to cubic crystal family. It can be seen as two interpenetrating face-centred-cubic (fcc) sub-lattices with one sub-lattice displaced from the other by one quarter of a distance along a diagonal of a cube, that is, a displacement of a √3/4 [5]. The planar density (PD) of atoms on the Si (100) and Si (110) and Si (111) surface can be calculated by knowing the number of atoms on the plane and dividing by the area of the plane. The lattice constant for Si is 0.543 nm denoted by 'a'. The number of atoms on the three faces are 2 on each face, and the areas of the planes are a^2, a√ 2a, and {(1/2) x (√2a) x ((√2a (√3/2)) = a^2√3/2}, giving PDs tabulated below in Table I. The area of a hexagonal plane is given by 2 times the area of a trapezoid having two parallel sides as 'a' and '2a' and a height of (a√3/2). This equals (3√3/2) a^2. PD for the hexagonal closely packed (hcp) crystal plane of 6H-SiC or 4H-SiC having (0001) surface orientation is therefore given as below in Table I where 'a' equals 0.3073 nm. The number of atoms in the 4H-SiC (1120) plane or a-face is 5/3, and the area of the plane is 'a' x 'c', where a = 0.3073 nm and c = 1.0053 nm for the 4H-SiC polytype. It can be observed that the density of atoms on 4H-SiC (0001) face is nearly the same as on Si (111) face. The comparison of N_f values in oxides on 4H-SiC MOS devices should therefore be made with those in oxides grown on Si (111) face. The PD on a clean semiconductor surface represents P_b centres

which act as surface recombination centres. These states on Si surface reduce to 10^{11}-10^{12}/cm^2 after oxidation [2, 6].

Table I. Planar density of atoms on the Si cubic faces and on 6H- and 4H-SiC (0001) hcp faces.

Si(100) (x 10^{14}/cm^2)	Si(110) (x 10^{14}/cm^2)	Si(111) (x 10^{14}/cm^2)	6H-or 4H-SiC (0001) hcp plane (x 10^{14}/cm^2)	4H-SiC (1120) hcp plane (x 10^{14}/cm^2)	Ratio of PD Si(111) / Si(100)	Ratio of PD Si(100) / Si(110)	Ratio of PD of 4H-SiC (0001) / Si(111)	Ratio of PD of 4H-SiC (0001) / Si(100)
6.7	4.8	7.8	8.1	5.4	1.16	1.4	1.04	1.21

In MOS devices on semiconductors such as Si and SiC, the upper half of the bandgap has acceptor type interface states and the lower half has donor type of interface states [7]. Oxidised Si (111) has shown donor type interface states in the upper half of the bandgap also [8]. Donor states at the semiconductor/insulator interface are neutral when filled with electrons and become positive after donating electrons (empty) or capturing holes. In the p-type MOS device, the Fermi level is close to the VB. The donor states are empty and are therefore positive. They can represent positive charge in the p-type MOS device coming from donor states. Acceptor states at the semiconductor/insulator interface are negative when filled with electrons and become neutral after donating the electrons (empty). In the n-type MOS device, the Fermi level is close to the CB. The acceptor states are filled and are therefore negative. They can represent negative charge in the n-type MOS device coming from acceptor states. Fixed charges in MOS devices could be positive or negative. They do not exchange charge with the CB. In Si, they can come from Si-O bonded excess Si and are usually positive only due to incomplete oxidation [9]. In SiC, they can come from Si-C-O bonded excess Si or C and O. Excess Si will give positive charges, such as in p-MOS device on 4H-SiC-Si-face [10-11] and excess C will give negative charges in MOS device, such as in C-face of 4H-SiC [12]. The observed low-field leakage current in this device of 10^{-8}A/cm^2 is more than the oxide displacement current of 5 x 10^{-9}A/cm^2 indicating the absence of NITs and presence of bulk defects due to carbon [12-14]. Absence of NITs on the C-face of 4H-SiC results in large surface mobility of about 118cm^2/V-s but has a low oxide breakdown of about 5MV/cm due to large number of negative fixed charges and bulk defects mainly due to excess carbon.

Before discussing the correlation of positive charge densities and border trap densities in the Si/SiO_2 and the 4H-SiC/SiO_2 systems, the electrically inactive fixed charges and the three types of interface traps existing in the SiC/SiO_2 system are distinguished. They are tabulated below in Table II. One is at the interface only, and arises from the so-called P_b centres or P_{bC} centres [15]. A P_b centre is Si atom connected to three Si atoms at the interface with one dangling bond or a dangling bond on the second Si atom connected to the Si atom below it. These are known as P_{b0} and P_{b1} in the Si Science and Technology where their density is about 10^{12}/cm^2 to 10^{13}/cm^2 on the p-Si (111) surface [16]. The density of P_{b1} is less than the density of P_{b0}. The P_{b0} centre on Si (111) is just denoted as P_b centre [15]. The P_{bC} centres are carbon-dangling bonds on the 4H-SiC surface. There density is found to be 3-4 x 10^{12}/cm^2 [17]. The Si/SiO_2 system has only P_b centres but the SiC/SiO_2 system has both P_b and P_{bC} centres due to Si and C dangling bonds. They can acquire a positive or negative charge and are therefore amphoteric. There is another type of interface traps in the SiC/SiO_2system that arise due to sp^2-bonded carbon clusters and graphite-like carbon [18]. These are mainly donor states or hole traps in the lower half of the SiC bandgap with the intrinsic Fermi level shown to be at E_c-0.97 eV in 4H-SiC due to intrinsic defect density of 1.1 x 10^{14}/cm^3 [19-20]. Being donor states, they are neutral when occupied with electrons and become positive upon donating an electron or capturing a hole. These add positive charges to p-type MOS device when the Fermi level is near the VB and when the donor states are empty and therefore positively charged. Donor states due to sp^2 bonded carbon and graphite like carbon are reduced in number because they are oxidised in oxygen ambient. High temperature inert anneal in N_2 or Ar gas has high density of donor states and low temperature inert anneal has low density of donor states, so N_f is accordingly higher or lower due to inert anneals [21-23]. The small upper half of the 4H-SiC bandgap of 0.97 eV above the intrinsic Fermi level also has acceptor states coming from sp^2 bonded carbon and graphite like carbon that have been shown to be passivated by NO annealing and add to the traps near VB after being passivated with N [24]. The acceptor states are negative when occupied and neutral when empty. The donor states occupy almost two-thirds of the 4H-SiC bandgap below the intrinsic Fermi level are much larger in density with the sp^2 bonded carbon states starting from E_v + 1.4 eV [18]. The above two types of interface traps are represented as D_{it}. The contribution to D_{it} from the P_b centres is not observed in Si-face of 4H-SiC/SiO_2system by Afanasev et al. [18]. However, after wet re-oxidation [10], the donor states are reduced and acceptor states are increased as observed in Fig. 2 of the report by Williams et al. [24] making the D_{it} distribution asymmetric after re-oxidation. The third type of traps at the SiC/SiO_2 interface are called "border" traps, which are present in the oxide within about 3 nm of the interface and can exchange charge with the Si or SiC CB [3-4]. These are represented as D_{bt} or D_{NIT}. It is difficult to distinguish between the three types of traps by electrical characterisation methods except

the fact that border traps are dominant at low frequencies of less than 100 Hz [25-26]. It is to be noted that D_{it} at E_c-0.2 eV is not necessarily the same as D_{NIT} near CB of the semiconductor unless D_{it} is passivated substantially. In the as oxidised dry or wet oxide on Si-face of 4H-SiC having (0001) orientation, the D_{it} at E_c-0.2 eV is at 24 x 10^{11}/cm^{2}eV with Ar annealing gas containing small parts of oxygen [24, 27]. Wet re-oxidation at 950^{o}C for 3 hrs has shown to reduce the donor states and increase the acceptor states as mentioned earlier [24].

Table II. Switching and Fixed states in Si and SiC MOS devices

Semiconductor	Interface Switching States that exchange charge with CB or VB			Fixed charges that do not exchange charge with CB or VB
Si (111)	P_{b0} denoted as P_b only.		Donor type border traps near CB, Si-O-O-O	Si-O
4H-SiC-Si-(0001)	P_{b0}, P_{b1}, P_{bC}	sp^2-bonded carbon and graphite	Acceptor type border traps near CB, Si-C-O-O	Si-C-O

III. Results and Discussion

It is observed that the dry oxidation of n-type Si-face 4H-SiC or 6H-SiC surfaces followed by inert anneal in pure Ar gives a high density of sp^2 bonded carbon and graphite-like states at the oxide/SiC interface that is shown as negative acceptor states giving high negative fixed charge density due to the deep traps. A 10^{20}/cm^3 carbon is detected [27]. It has been pointed out that acceptor states show up as negative fixed oxide charges in the n-type MOS device with the Fermi level close to the CB and all the states below the Fermi level being occupied with electrons. The high temperature dry oxidation with pure Ar anneal at high temperature does not form significant border traps as can be observed in Fig. 2 of the study by Williams et al. indicating a very small 'hump' at about E_v + 2.7 eV [1, 24]. Annealing the pure Ar annealed device in low partial pressure of O_2 (0.001% O_2) at 1500^{o}C for 1 minute removes a lot of the carbon to 10^{18}/cm^3 level thereby reducing the acceptor states or the negative charges in the n-MOS device [27]. The 1MHz high frequency C-V curve shifts left. Some positive charge remains which is due to Si-C-O bonded excess Si in the MOS device. These charges are electrically inactive and the N_f obtained is 12 x 10^{11}/cm^2 [27]. Similar observation is made on the MOS device on Si-face of 6H-SiC by Tyagi et al. [28], although 6H-SiC MOS device has less acceptor states near CB. The above analysis deals with removal of carbon to remove negative charges or indirectly add positive charges, shifting the C-V curves to the left. Now, consider the case of wet oxidation to fabricate an n- type MOS device. After wet oxidation followed by inert anneal in Ar, the sp^2 bonded carbon states are present as before giving negative N_f value of -12 x 10^{11}/cm^2. When this oxide is wet re-oxidised at low temperature of 950^{o}C for 3 hrs, the acceptor states increase further to more negative values because of formation of high density of border traps in the form of Si-C-O-O correlated bonds sometimes called as 'rechargeable' E' centres [29]. That is, there is addition of O atoms instead of removal of C atoms. The high frequency C-V curve now shifts further to the right giving higher value of N_f of -24 x 10^{11}/cm^2 due to negative charges forming border traps. Essentially, removal of C shifts the C-V curve to the left by reducing acceptor states and addition of O shifts the C-V curve to the right by adding more acceptor states [1, 10]. The positive charge density due to fixed charges from Si-C-O bonds is identified by the fact that before wet re-oxidation N_f was 24 x 10^{11}/cm^2 in the p-type MOS device half of which were due to donor states in the lower half of the band gap and show up as positive charges in the p-type MOS device. After wet re-oxidation the N_f of 24 x 10^{11}/cm^2 becomes only 12 x 10^{11}/cm^2 implying that 12 x 10^{11}/cm^2 charges have been removed which were Si-C-O bonded positive charges in the initial wet oxidised p-type 4H-SiC MOS device and 12 x 10^{11}/cm^2 density of border traps are created with the addition of O having associated equal positive charge from the same neutral oxygen vacancies [1, 10]. Similar observation is made by Yano et al. with a difference that forming gas anneal is performed post-metallization which is discussed later [11]. It is to be noted that the positive charge density on the n-type and p-type device after dry or wet oxidation is 12 x 10^{11}/cm^2. These are Si-C-O bonded excess Si based positive charges which are electrically inactive. They do not exchange charge with the SiC CB. In the Si/SiO_2 system, the density of positive charges is found to be 4 x 10^{11}/cm^2 as shown by the study of Deal et al. [2]. It can be observed that carbon is replaced by Oxygen in the Si/SiO_2 system. Oxygen has two more electrons as compared to carbon reducing the positive charge density three times to 4 x 10^{11}/cm^2 in the Si/SiO_2 system. A further inert annealing in N_2 or Ar ambient reduces the positive charge density to 2 x 10^{11}/cm^2 as per the 'Deal triangle' [2]. It is thus observed that the positive fixed charge density in 4H-SiC/SiO_2 as well as Si/SiO_2systems are completely correlated considering fast pullout of samples from the wet oxidising ambient [2]. A lower bound of ~3 x 10^{11}/cm^2 is estimated as the density of border traps in the Si/SiO_2 system [3-4]. This translates to ~12 x 10^{11}/cm^2 for the 4H-SiC/SiO_2system when Carbon with two less electrons adds three times more positive charges to the traps. Thus, the density of border traps or near interface traps (NITs) in Si/SiO_2system are also correlated to the density of border traps in the 4H-SiC/SiO_2system. Considering E' centre as the constituent of border traps, where Si-C-O-O is the 'rechargeable' E' centre [29] in the 4H-SiC/SiO_2 system has D_{NIT} of 24 x

$10^{11}/cm^2eV$ after NO annealing [1]. D_{NIT} will be 12 x $10^{11}/cm^2$ eV before NO annealing. Si-O-O-O is the 'rechargeable' E' centre in the Si/SiO_2system having a density of 4 x $10^{11}/cm^2eV$ due to the presence of O in place of C that reduces the trap density three times. A lower bound of ~3x$10^{11}/cm^2$ is determined for the Si/SiO_2 system as mentioned earlier [3-4].

Table III. Fixed charge density N_f, and interface trap density D_{it} at E_c-0.2 eV, at different oxide annealing ambient on n-SiC-Si-face MOS device.

n-type SiC-MOS device, Oxide Annealing temperature (^oC)	Oxide Annealing ambient % O_2	Oxide Annealing Time (minutes)	Fixed charge density, N_f ($x10^{11}/cm^2$)	Interface trap density at E_c-0.2 eV D_{it} ($x10^{11}/cm^2eV$)
1100	Small parts O_2 in Ar	30	-12(adds O)	24
950	Wet re-ox	3 hrs	-24(adds O further)	60
1300	0.001	1	-3(removes sp2 C)	49
1300	0.1 (like re-ox)	1	-12 (adds O)	49
1500	Pure Ar	1	-24(adds sp2 C)	62
1500	0.001	1	+12(removes sp2 C)	24
1500	0.1 (like re-ox)	1	-16 (adds O)	63

Table IV. Fixed charge density N_f, and interface trap density D_{it} at E_c-0.2 eV, at different oxide annealing ambient on n- and p-4H-SiC-Si-face MOS devices in the order of 1MHz High Frequency C-V curve shifts.

n-type SiC-MOS device, Oxide Annealing temperature (^oC)	Oxide Annealing ambient % O_2	Detected carbon cm^{-3} (cm^{-2} for 2 nm interface)	Oxide Annealing Time (minutes)	Fixed charge density, N_f in p-type MOS device ($x10^{11}/cm^2$)	Fixed charge density, N_f in n-type MOS device ($x10^{11}/cm^2$)	Shift in 1MHz High Frequency C-V curve	Interface trap density at E_c-0.2 eV D_{it} ($x10^{11}/cm^2eV$)
1500	Pure Ar	10^{20} (2 x 10^{13})	1		-24(adds sp2 C)		62
1300	0.001		1		-3(removes sp2 C)	left	49
1500	0.001	10^{18} (2 x 10^{11})	1		+12(removes sp2 C, excess Si)	Further left	24
1100	Small parts O_2 in Ar		30	24	-12(adds O, but no change in D_{it}, excess O)	Right	24
1300	0.1 (like re-ox)		1		-12 (adds O, increases D_{it})	Same as previous	49
1500	0.1 (like re-ox)		1		-16 (adds O, increases D_{it} further)	Further Right	63
950	Wet re-ox		3 hrs	12	-24(adds O further, increases D_{it} further also)	Further right	72

The data presented in Table III and IV is analysed next. In Table III it is shown that 1 minute anneal at the same temperature of 1300^{o}C or 1500^{o}C with larger partial pressure of oxygen (at 0.1%) acts like a re-oxidation process giving higher negative N_f in the n-type MOS device. Higher negative N_f represents higher density of near interface traps or D_{NIT}. Higher temperature of 1500^{o}C also gives higher interface trap density D_{it}, implying higher concentration of carbon at the interface. The N_f and D_{it} data of Table III which is obtained from the study of Kobayashi et al. [26] is rearranged in Table IV along with the N_f and D_{it} data from the study of Chung et al. [10] in the order of left and right shifts of the 1MHz high frequency C-V curves that represents removal of carbon and addition of oxygen at the SiC/SiO_2 interface. D_{it} is 8 x $10^{11}/cm^2$ eV at E_v + 0.2 eV as shown in Fig.2 of Williams [24]. Si-C-O-O E' centres in wet re-oxidised SiC MOS sample have one unpaired electron on the Si atom in each one of them. If 1N replaces 1O, then a positive charge is added and an E' centre becomes neutral. The N_f after NO annealing in n-MOS device therefore becomes zero whereas the positive charge doubles. Carbon is reduced to 2 x $10^{11}/cm^2$ at the interface with 0.001% O_2 ambient at 1500^{o}C for 1 min as presented in Table IV. Since Carbon has 4 valence electrons, each one can contribute to the interface state charge. Therefore, carbon states at the VB edge become 4 x 2 x $10^{11}/cm^2$ eV which equals 8 x $10^{11}/cm^2eV$ as can be seen in Fig.2 of Williams et al. [24]. Similarly, Si-C-O-O has (4+4+2+2) bonded valence electrons equalling 12. Each of them can contribute to the interface state giving D_{it} of 12 x 2 x $10^{11}/cm^2eV$. This equals D_{it} of 24 x $10^{11}/cm^2eV$ near the CB edge at E_c-0.2 eV. This is the minimum D_{it} achievable. After wet re-oxidation at 950^{o}C for 3 hrs, the D_{it} is 72 x $10^{11}/cm^2eV$. This means that the carbon content has gone up to

72/12 equals 6 x 10^{11}/cm^{2}at the SiC/SiO_2 interface. This also means that the volume density at the interface is now 3 x 10^{18}/cm^3 for a 2 nm interface. It can be concluded that low temperature re-oxidation for a long time of 3hrs tends to increase the carbon density at the interface. The charges in the MOS devices fabricated on n- and p-type (111) oriented Si surface are usually positive and therefore only positive charges obtained on the 4H-SiC MOS devices fabricated on the n- and p- (0001) oriented surfaces are correlated with those in the MOS devices fabricated on Si (111) surfaces. Also, the border traps in Si/SiO_2 and 4H-SiC/SiO_2system are correlated. Having negative acceptor N_f in n-type MOS device implies more carbon at the interface even if it is occurring with the addition of oxygen. This can be observed in Table IV, where the higher D_{it} at E_c-0.2 eV is related to higher negative N_f values in the n-MOS devices indicating higher carbon content at the interface as explained earlier.

Observing data in Table IV informs the author that if D_{it} and D_{NIT} is low near the CB without NO annealing as determined from the n-type MOS device, then the fixed charges N_f in the p-type MOS device is higher due to higher density of donor states and therefore leakage current and oxide breakdown is lowered for the n-channel MOSFET due to increase in the cathode field for electron tunnelling [14]. The switching states are converted to fixed states. If the N_f in the p- and n-type devices is observed then it can be concluded that the difference in N_f is the same at 36 x 10^{11}/cm^2. N_f after oxidation at 1100^{o}C followed by inert Ar anneal for 30 min is 24x10^{11}/cm^2 in the p-type device and -12 x 10^{11}/cm^2 in the n-type device. This study by Chung et al. [10] shows that after wet re-oxidation at 950^{o}C for 3 hrs, N_f in the p-type device reduces to 12x10^{11}/cm^2, but N_f in the n-type device increases to -24x10^{11}/cm^2, keeping the same difference in N_f at 36x10^{11}/cm^2. It has also been observed that reducing D_{NIT} with high temperature oxidation increases D_{it} at E_c-0.2 eV, and D_{NIT} is doubled after NO annealing in the n-type device along with fixed states in the p-type device [1]. It can be inferred from the above observations and analysis that N_f in the p-type MOS device annealed at 1300^{o}C in 0.001% O_2 as shown in the Table IV will be about 33x10^{11}/cm^2 which will increase the low-field leakage current and high-field tunnelling current and thus lower the breakdown field in the oxide [14]. After NO annealing this N_f will double to 66x10^{11}/cm^2 in the p-type device increasing the leakage current and lowering the oxide breakdown field further. Observing the 1500^{o}C annealing temperature having 0.1% O_2 in the ambient as shown in Table IV, N_f in the p-type device would be 20x10^{11}/cm^2 which after NO annealing would double and lower surface mobility and oxide breakdown field. N inclusion at the interface is desirable to reduce D_{it} to much lower levels from the pre-NO annealed state for improving surface effective and field effect (FE) mobility. It seems that wet re-oxidation needs to be done to reduce D_{NIT} to 12 x 10^{11}/cm^2 before NO annealing as shown in the p-type device. This will increase to 24x 10^{11}/cm^2 after NO annealing. Since the charges have been shown to correlate to the Si/SiO_2 system, not much can be done further to increase mobility of n-channel 4H-SiC MOSFET fabricated on Si-face of (0001) oriented surface without sacrificing oxide breakdown field [14]. The window of ΔN_f in p-type and n-type MOS device of 36x10^{11}/cm^2 before NO annealing informs the author that not much can be done to reduce this window. If the window is more to the left then the fixed states in the p-type device is higher which increases the leakage current and lowers the oxide breakdown field as explained earlier that the switching states are converting to fixed states [1, 14]. If the window is more to the right, the D_{NIT} and D_{it} is higher which lowers the surface mobility, although the fixed charges due to D_{NIT} in the n-type device will neutralise by inclusion of N while D_{it} is reduced by one order throughout the bandgap [10, 24, 30]. It can also be inferred that one-third of the window represents the density of E' centres near the SiO_2/Si(111) at 12 x 10^{11}/cm^2 due to the absence of carbon and indicates better interface abruptness [31]. This density closely matches the density of E' centres reported in Fig. 16 of a 1998 review article that promotes MOS/EPR studies [32]. Oxidised Si (111) has donor states in the upper half of the Si band gap also [8]. They therefore show up as positive charge in p-type MOS device and are neutral in n-type MOS device. One data set in Deal's 1967 study shown in Table III (A) of his reference [2], shows N_f of 10 x 10^{11}/cm^2 when p-Si (111) is annealed at 550^{o}C in O_2 ambient for 90 minutes. Long-time low temperature re-oxidation results in 'rechargeable' E' centres of the order of low 10^{12}/cm^2.along with electrically inactive excess Si. Oxidised 4H-SiC Si-face-(0001) has acceptor states in the upper half of the band gap [1, 10]. They therefore show up as negative charges in n-type MOS device. They are neutral when empty in p-type MOS device.

The window of N_f is smaller as obtained by Yano et al. [11]. It is 29x10^{11}/cm^2 for wet oxidation/Ar annealing and 22x10^{11}/cm^2 for dry/wet re-oxidation/Ar annealing or wet/wet re-oxidation/Ar annealing. It is to be noted that the oxidation temperature for Yano is 1150^{o}C as compared to 1100^{o}C for Chung et al. [10], although the final temperature is the same at 950^{o}C due to wet re-oxidation for both. Why is Yano et al. [11] getting a smaller window of ΔN_f? Forming gas annealing could be one thing. Yes it is. Forming gas annealing as post-metallization annealing is performed by Yano et al. [11] but not by Chung et al. [10]. H attaches to Si-

C-O-O E' centres and Si-C-O bonded positive charges at the interface. It changes the distribution from 12 +12 in Chung's study to 19 +6 in Yano's study for the p-type MOS device where19 x $10^{11}/cm^2$ charges come from the deep states and 6 x $10^{11}/cm^2$ charge density comes from the electrically inactive excess Si based charges. It can be observed that Si-C-O-O-H bonded deep traps have (4+4+2+2+1) bonded valence electrons. Since minimum carbon density is found to be 2 x $10^{11}/cm^2$at the SiC/SiO_2 interface, therefore the trap density becomes 13 x 2 x $10^{11}/cm^2$ equalling 26 x $10^{11}/cm^2$. Two-thirds of this density forms donor traps in the lower half of the band gap giving a trap density of about 18 x $10^{11}/cm^2$. The author believes that after wet re-oxidation followed by H attachment due to forming gas anneal, the positive charge of the associated E' centre formed after re-oxidation becomes negative giving N_f of -12x$10^{11}/cm^2$ in the p-type device. For the n-type device, N_f is -4 x $10^{11}/cm^2$ (~6 for D_{NIT} which is half of 12 x $10^{11}/cm^2$ due to addition of an electron to the E' centre) and changes by -12 to -17x$10^{11}/cm^2$ after wet re-oxidation. This -12 x $10^{11}/cm^2$ change in N_f is the same in Chung's as well as Yano's study related to the formation of deep acceptor traps or NITs. The window in ΔN_f is therefore 25-(-4) = 29 x $10^{11}/cm^2$ between the p-type and n-type MOS devices before re-oxidation. After wet re-oxidation, the window in ΔN_f becomes 6-(-17) = 23x$10^{11}/cm^2$. This is because in the p-type device N_f is reduced to 6 due to an electron attachment from H, and in the n-type device (-12 to -24 shift) has become (-4 to -17 shift), although the shift is the same in both meaning that the D_{NIT} formed is the same amount due to re-oxidation. The study by Chung et al. [10] and Yano et al. [11] are similar with the difference that forming gas annealing is not performed by Chung et al. [10]. High temperature dry N_2 or Ar annealing gives much larger D_{it} at E_c-0.2 eV at 60-100x $10^{11}/cm^2eV$. With some oxygen present it can come down to 24-50x$10^{11}/cm^2eV$ with 24x$10^{11}/cm^2eV$ appears to be minimum achievable as shown in Table IV. The high temperature annealing or oxidation at 1300°C or 1500°C has the disadvantage of keeping the processing time short to maximum a few minutes that could affect reproducibility of the N_f and D_{it} charge and interface trap densities. The benefits and advantages of power electronic circuits and systems built on wide bandgap silicon carbide compound semiconductor are highlighted in a recent invited IEEE article [33].

IV. Conclusion

The positive charge density due to excess Si in the wet oxidised/wet re-oxidised/Ar annealed n-type and p-type 4H-SiC MOS device on (0001) oriented Si surface is completely correlated to the positive charge density due to excess Si in the wet oxidised Si MOS device on (111) oriented surface. The density of positive charges in the 4H-SiC MOS device of 12 x $10^{11}/cm^2$ is three times the density of positive charge in the Si-MOS device which is 4 x $10^{11}/cm^2$. The addition of carbon in the Si-C-O bonded excess Si has two less electrons so as to bring about a three times change in the positive charge density. Similarly, the border trap density in the Si MOS device is correlated to the D_{NIT} in the 4H-SiC MOS device. The lower bound on the border trap density in Si MOS devices is ~3 x $10^{11}/cm^2eV$. This density is about three times less than D_{NIT} in the 4H-SiC MOS device at 12 x $10^{11}/cm^2eV$. A ΔN_f window of 36 x $10^{11}/cm^2$ is observed between the p-type and n-type 4H-SiC MOS device. A left shift of this window through high temperature processing will increase the fixed positive charge density in the p-type MOS device coming from deep traps. It will further increase after the desirable NO annealing. This will result in higher leakage current and lower oxide breakdown field. The switching states convert to fixed states. A right shift of the window causes the D_{NIT} to increase, that lowers the surface mobility in the n-channel 4H-SiC MOSFET. Higher interface trap density represent higher carbon content at the SiC/SiO_2 interface.

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